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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/801,812	02/14/1997	JOHN H. GIVENS	2269-6888US(1995-1078.00/	6774

63162 7590 05/14/2008

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EXAMINER	
MALDONADO, JULIO J	

ART UNIT	PAPER NUMBER
2823	

NOTIFICATION DATE	DELIVERY MODE
05/14/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTOMail@traskbritt.com

Office Action Summary	Application No.	Applicant(s)	
	08/801,812	GIVENS, JOHN H.	
	Examiner	Art Unit	
	JULIO J. MALDONADO	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,9-15 and 64-66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6, 9-15 and 64-66* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The rejection of claims 1-6, 9-15 and 64-66 is withdrawn in further review of the prior art of record.

2. A new rejection is included in this office action.

3. Claims 1-6, 9-15 and 64-66 are pending in the application.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4, 6, 9-14 and 64 are rejected under 35 U.S.C. 103(a) as being unpatentable over deSilva (U.S. 5,926,736) in view of Mizobuchi et al. (U.S. 5,990,556, hereinafter Mizobuchi) and Fiordalice et al. (U.S. 5,420,072, hereinafter Fiordalice).

In reference to claims 1, 3, 4, 6, 9, 12, 13 and 64, deSilva (Figs.1-5) teaches a method of forming an interconnect structure including the steps of forming a recess (106, 112) within a dielectric material (102) situated on a substrate (100), the recess (106, 112) extending below a top surface of the dielectric material (102); forming a diffusion barrier layer (116) substantially conformally on the top surface of the dielectric material (102) and over an interior surface of the recess (106, 112); forming an electrically conductive layer (118) on the barrier layer (116) over the top surface of the

dielectric material (102) and substantially within the recess (106, 112) such that voids (120, 122) are present within the recess; forming an energy absorbing layer (124) on the electrically conductive layer (118), the energy absorbing layer (124); and utilizing a furnace to apply energy to the energy absorbing layer (124) sufficient to cause the electrically conductive layer (118) to fill the voids (120, 122) within the recess (120, 122) (deSilva, column 2, line 30 – column 5, line 30).

Furthermore, deSilva teaches wherein the barrier layer is made of titanium (deSilva, column 2, lines 54 – 63), the conductive material is made of aluminum (deSilva, column 2, lines 66 – 67) and wherein the energy absorbing layer is made of titanium nitride (deSilva, column 3, lines 5 – 10).

deSilva fails to dislcose wherein said substrate is a semiconductor substrate; forming a seed layer on the diffusion barrier layer over the top surface of the dielectric material and within the recess, the diffusion barrier layer comprising a material having a melting point greater than or equal to that of a material comprising the seed layer, wherein the material comprising the seed layer is made of aluminum, titanium nitride, titanium, titanium aluminide or comprises tungsten, wherein the seed layer and the barrier layer are formed by a chemical vapor deposition process.

However, Mizobuchi (Figs.26-27) teaches a method of forming an interconnect structure including the steps of providing a semiconductor substrate (1); forming a dielectric layer (3) having a contact hole (4); forming a barrier layer (31) within said contact hole (4), wherein said barrier layer is selected from a variety of materials, including TiW, TiN and tungsten; forming a seed layer (33) over said barrier layer (31),

wherien said seed layer is formed by chemical vapor deposition and is made of W; and forming a contact layer (12) made of aluminum (Mizobuchi, column 7, line 25 – column 8, line 65).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of deSilva and Mizobuchi to enable including the barrier layer and the seed layer over the barrier layer in deSilva according to the teachings of Mizobuchi because this would result in an a low resistance interconnect structure, and reduced aluminum diffusion (Mizobuchi, column 3, line 24 – column 4, line 5).

The combined teachings of deSilva and Mizobuchi fail to dislcose removing portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material.

However, Fiordalice (Figs.1-8) teaches a method to form an interconnect structure including the steps of forming a recess (16) within a dielectric material (14) situated on a semiconductor substrate (12), the recess extending below a top surface of the dielectric material (14); forming a layer made to titanium (not shown) within said recess and on the surface of said dielectric material (14), wherein said titanium layer is labeled a titanium barrier layer; forming a titanium nitride layer (22, 24) on the top surface of the dielectric material (14) and over an interior surface of the recess (16), wherein said titanium nitride layer (22, 24) is made of titanium nitride by a chemical vapor deposition process; forming an electrically conductive layer (26) made of aluminum on the seed layer (24) over the top surface of the dielectric material (14) and

within the recess (16); and removing portions of the electrically conductive layer (26) that are situated above the top surface of the dielectric material (14) by a chemical mechanical polishing process (Fiordalice, column 2, line 21 – column 5, line 34).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of deSilva and Mizobuchi with Fiordalice to enable removing overlying layers above the dielectric layer of deSilva and Mizobuchi according to the teachings of Fiordalice because the patterning steps are disclosed by Fiordalice to be standard photolithographic patterning and etching steps in forming interconnect structures (col.4, lines 40-50) and the patterning steps would amount to no more than the predictable use of the standard steps to achieve the established function of forming interconnect structures.

In reference to claim 2, the combined teachings of deSilva, Mizobuchi and Fiordalice teach wherein forming a diffusion barrier layer comprises forming the diffusion barrier layer by chemical vapor deposition (Fiordalice, column 2, line 56 – column 3, line 63).

In reference to claim 6, the combined teachings of deSilva, Mizobuchi and Fiordalice teach depositing tungsten by a chemical vapor deposition process (Fiordalice, column 4, lines 51 - 66).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to enable forming the tungsten seed layer using the deposition process in the combination of deSilva, Mizobuchi and Fiordalice because one of ordinary skill in the art would have been motivated to look to analogous art teaching

alternative suitable or useful methods of forming the disclosed seed layer and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

In reference to claim 14, the combined teachings of deSilva, Mizobuchi and Fiordalice substantially teach all aspects of the invention but fail to expressly disclose wherein the recess has an aspect ratio greater than about four to one. However, one of ordinary skill in the art would have been led to the recited dimensions through routine experimentation and optimization to obtain a desired contact opening. Applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966). See also MPEP 2144.04(IV)(B).

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over deSilva ('736) in view of Mizobuchi ('556) and Fiordalice ('072) as applied to claims 1-4, 6, 9-14 and 64 above, and further in view of Taguchi (U.S. 6,306,761 B1).

The combined teachings of deSilva, Mizobuchi and Fiordalice teach wherein the barrier layer is made of titanium nitride (Mizobuchi, column 7, lines 53 – 58).

The combined teachings of deSilva, Mizobuchi and Fiordalice fail to disclose prior to forming a seed layer on the diffusion barrier layer, heating the diffusion barrier layer in an environment substantially containing a nitrogen gas.

However, Taguchi teaches a method of forming a contact structure including forming a barrier layer made of titanium nitride, and densifying said barrier layer on the barrier layer by lamp annealing said titanium nitride layer in a N_2 atmosphere at a temperature of 800^{o}C for 60 seconds, said process performed prior to performing further deposition steps (Taguchi, column 10, lines 10 – 46).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of deSilva, Mizobuchi and Fiordalice with Taguchi to enable performing a heat treatment in the titanium nitride layer of the combination of deSilva, Mizobuchi and Fiordalice according to Taguchi for the further advantage of enhancing the barrier layer properties of the titanium nitride layer (Taguchi, column 10, lines 40 – 45).

7. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over deSilva ('736) in view of Mizobuchi ('556) and Fiordalice ('072) as applied to claims 1-4, 6, 9-14 and 64 above, and further in view of Yim (U.S. 5,869,395).

The combined teachings of deSilva, Mizobuchi and Fiordalice substantially teach all aspects of the invention but fails to disclose wherein the recess comprises a contact

hole situated below a trench, wherein said semiconductor substrate has a lower substrate and terminates at an opposite end thereof at said trench, and wherein said trench extends from said opposite end of said contact hole to a top surface of said dielectric material and parallel to the plane of the lower substrate.

However, Yim (Figs.2A-2K) in a related method to form an interconnect structure teaches the steps of depositing titanium nitride by a chemical vapor deposition process; using chemical-mechanical polishing to remove portions overlaying a damascene trench formed on a dielectric layer (210); providing a recess comprising a contact hole (260) situated below a trench (240); providing a semiconductor substrate (200) having a lower substrate (202) and terminating at an opposite end thereof at said trench (240), wherein said trench (240) extends from said opposite end of said contact hole (260) to a top surface of said dielectric material (210), and parallel to the plane of the lower substrate (202) (Yim, column 4, line 26 – column 7, line 31).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of deSilva, Mizobuchi and Fiordalice with Yim to enable forming the interconnect structure of the combination of deSilva, Mizobuchi and Fiordalice according to the teachings of Yim because one of ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or useful methods of forming the disclosed interconnect structure the combination of deSilva, Mizobuchi and Fiordalice and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

8. Claims 65 and 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over deSilva ('736) in view of Fiordalice ('072).

deSilva (Figs.1-5) teaches a method of forming an interconnect structure including the steps of forming a recess (106, 112) within a dielectric material (102) situated on a substrate (100), the recess (106, 112) extending below a top surface of the dielectric material (102); forming a diffusion barrier layer (116) substantially conformally on the top surface of the dielectric material (102) and over an interior surface of the recess (106, 112); forming an electrically conductive layer (118) on the barrier layer (116) over the top surface of the dielectric material (102) and substantially within the recess (106, 112) such that voids (120, 122) are present within the recess; forming an energy absorbing layer (124) on the electrically conductive layer (118), the energy absorbing layer (124); and utilizing a furnace to apply energy to the energy absorbing layer (124) sufficient to cause the electrically conductive layer (118) to fill the voids (120, 122) within the recess (120, 122) (deSilva, column 2, line 30 – column 5, line 30).

Furthermore, deSilva teaches wherein the barrier layer is made of titanium (deSilva, column 2, lines 54 – 63), the conductive material is made of aluminum (deSilva, column 2, lines 66 – 67) and wherein the energy absorbing layer is made of titanium nitride (deSilva, column 3, lines 5 – 10).

deSilva fails to disclose wherein said substrate is a semiconductor substrate; forming a seed layer on the diffusion barrier layer over the top surface of the dielectric material and within the recess, the diffusion barrier layer comprising a material having a

melting point greater than or equal to that of a material comprising the seed layer, wherein the material comprising the seed layer is made of aluminum, titanium nitride, titanium or titanium aluminide; and removing portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material.

However, Fiordalice (Figs.1-8) teaches a method to form an interconnect structure including the steps of forming a recess (16) within a dielectric material (14) situated on a semiconductor substrate (12), the recess extending below a top surface of the dielectric material (14); forming a layer made to titanium (not shown) within said recess and on the surface of said dielectric material (14), wherein said titanium layer is labeled a titanium barrier layer; forming a titanium nitride seed layer (22, 24) on the top surface of the dielectric material (14) and over an interior surface of the recess (16), wherein said titanium nitride layer (22, 24) is made of titanium nitride by a chemical vapor deposition process; forming an electrically conductive layer (26) made of aluminum on the seed layer (24) over the top surface of the dielectric material (14) and within the recess (16); and removing portions of the electrically conductive layer (26) that are situated above the top surface of the dielectric material (14) by a chemical mechanical polishing process (Fiordalice, column 2, line 21 – column 5, line 34).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of deSilva and Fiordalice to enable providing the substrate of deSilva according to the teachings of Fiordalice because one of ordinary skill in the art would have been motivated to look to analogous art teaching

alternative suitable or useful methods and materials for the substrate of deSilva and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

It would also have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of deSilva and Fiordalice to enable including a titanium nitride seed in deSilva according to the teachings of Fiordalice because this would result in an interconnect structure with improved electro migration resistance (Fiordalice, column 1, lines 28 – 52).

Also, it would have been within the scope of one of ordinary skill in the art to combine the teachings of deSilva and Fiordalice to enable removing overlying layers above the dielectric layer of deSilva and Fiordalice according to the teachings of Fiordalice because the patterning steps are disclosed by Fiordalice to be standard photolithographic patterning and etching steps in forming interconnect structures (col.4, lines 40-50) and the patterning steps would amount to no more than the predictable use of the standard steps to achieve the established function of forming interconnect structures.

Response to Arguments

9. Applicant's arguments with respect to claims 1-6, 9-15 and 64-66 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JULIO J. MALDONADO whose telephone number is (571)272-1864. The examiner can normally be reached on Mon-Fri, 8:00 A.M.-4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571)-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/George Fourson/
Primary Examiner, Art Unit 2823

/J. J. M./
Examiner, Art Unit 2823